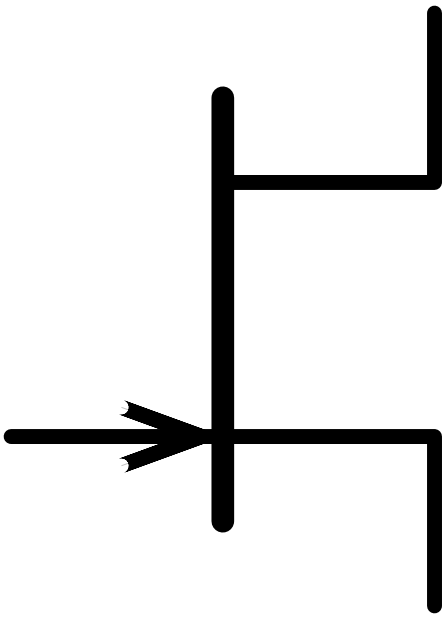
Calculating the voltage gain and output impedance of JFET amplifier stages



October 27, 2012

J.L.

This example shows how to evaluate the small-signal voltage gain and the output impedance of a junction field-effect transistor (JFET) amplifier stage. The output impedance will be evaluated using the results of Thévenin and Norton theorems. According to these theorems, the output impedance of any circuit stage is obtained as the quotient of open circuit voltage and short circuit current. The following analysis demonstrates how to apply both nodal and mesh analysis methods to JFET circuits.

The analysed circuit contains the JFET in a common-source configuration as shown in Figure 1. The analysis of other JFET amplifier configurations follow the same procedure as for the common-source amplifier.

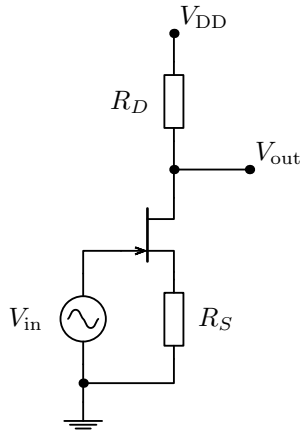
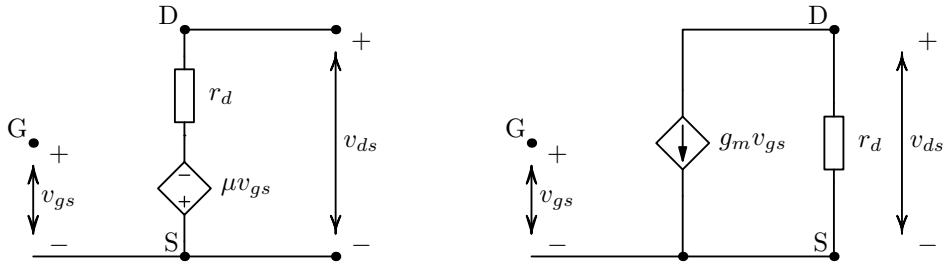


Figure 1: JFET amplifier in a common-source configuration

When considering input signals of small amplitudes, the JFET device can be modelled as a linear voltage-controlled source. Both voltage-controlled voltage source (VCVS) and voltage-controlled current source (VCCS) are suitable models for the JFET device, because the controlled source can be transformed accordingly using the Thévenin and Norton theorems of circuit analysis. Figure 2 indicates the VCVS and VCCS small-signal models for a general JFET device. These models are applicable only for audio frequencies, since the semiconductor pn-junction capacitances have been neglected to simplify the following analysis. The linear small-signal gain of the JFET is modelled by the amplification factor $\mu = g_m r_d$, where g_m is the internal transconductance and r_d the internal drain junction resistance.

The nodal method of analysis is first used for calculating the voltage gain transfer function of the common-source amplifier stage. The rules of the nodal analysis method require that all alternating (signal) sources in the cir-



(a) a voltage source model (b) a current source model

Figure 2: Controlled source models for a JFET device

cuit are represented as current sources. This requirement can usually be filled by applying the source transformations defined by the Norton and Thévenin theorems. Additionally, all the static DC sources are considered to behave as a ground node from the viewpoint of alternating signals. This is why all the wires originally connected to DC sources are reconnected to the ground node in the small-signal equivalent circuit.

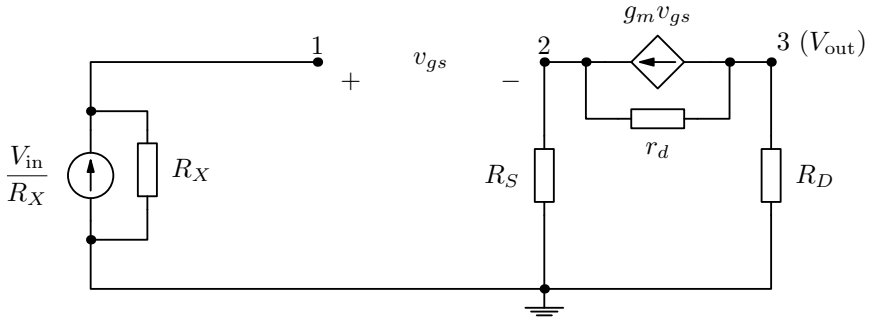


Figure 3: Voltage node model of the common-source amplifier

Figure 3 illustrates the equivalent circuit of the common-source amplifier of Figure 1, which is modified according to the rules of nodal analysis. Compared to the circuit shown in Figure 1, this small-signal model contains an additional resistor R_X. This resistor depicts the internal resistance of the signal source V_{in}, which is required to transform the voltage source to a current source. However, due to the infinite input resistance of the JFET, this additional source resistance will not affect the final results at all. The voltage nodes of the equivalent circuit 3 are indexed with numbers $1, 2$ and 3. The node 3 together with the ground node are the output terminals of the circuit. According to the rules of nodal analysis, the small-signal model of the common-source amplifier is represented mathematically by the matrix equation

$$\begin{bmatrix} \frac{1}{R_X} & 0 & 0 \\ 0 & \frac{1}{R_S}+\frac{1}{r_d} & -\frac{1}{r_d} \\ 0 & -\frac{1}{r_d} & \frac{1}{r_d}+\frac{1}{R_D} \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} \frac{V_{\text{in}}}{R_X} \\ g_m v_{gs} \\ -g_m v_{gs} \end{bmatrix}.$$

This matrix equation can be simplified by noting that the control voltage v_{gs} can be expressed as the difference of node voltages V_1 and V_2, namely $v_{gs} = V_1 - V_2$. Based on this observation, the transconductance terms can be moved from the output current vector to the admittance matrix side. This little trick will make the symbolic evaluation of the circuit much simpler. It should be noted that also in matrix equations when terms are moved to the other side of the equal sign the term changes its sign from positive to negative or vice versa. After transferring the transconductance terms from the current vector to the admittance matrix, the final form of the matrix equation is

$$\begin{bmatrix} \frac{1}{R_X} & 0 & 0 \\ -\frac{\mu}{r_d} & \frac{1}{R_S}+\frac{\mu+1}{r_d} & -\frac{1}{r_d} \\ \frac{\mu}{r_d} & -\frac{\mu+1}{r_d} & \frac{1}{r_d}+\frac{1}{R_D} \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} \frac{V_{\text{in}}}{R_X} \\ 0 \\ 0 \end{bmatrix}.$$

The output voltage can be solved systematically using Cramer's rule. An application of this rule yields a determinant division

$$V_3 = V_{\text{out}} = \frac{\begin{vmatrix} \frac{1}{R_X} & 0 & \frac{V_{\text{in}}}{R_X} \\ -\frac{\mu}{r_d} & \frac{1}{R_S}+\frac{\mu+1}{r_d} & 0 \\ \frac{\mu}{r_d} & -\frac{\mu+1}{r_d} & 0 \end{vmatrix}}{\begin{vmatrix} \frac{1}{R_X} & 0 & 0 \\ -\frac{\mu}{r_d} & \frac{1}{R_S}+\frac{\mu+1}{r_d} & -\frac{1}{r_d} \\ \frac{\mu}{r_d} & -\frac{\mu+1}{r_d} & \frac{1}{r_d}+\frac{1}{R_D} \end{vmatrix}},$$

which can be evaluated in symbolic form by applying the basic steps of solving a determinant in the numerator and the denominator. The solution of the determinant quotient for the node voltage V_3 is

$$V_3 = V_{\text{out}} = \frac{-V_{\text{in}}\mu R_D}{R_D + r_d + (\mu + 1)R_S}.$$

Form here one can obtain the transfer function

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-\mu R_D}{R_D + r_d + (\mu + 1)R_S}.$$

This result along with the short circuit current expression is later used for evaluating the formula for the output impedance of the common-source stage.

The analysis of the mesh currents requires its own small-signal equivalent circuit, which is obtained with slight modifications from the nodal analysis model. Basically all that is needed to reach the mesh-specific small-signal circuit is to transform the current sources to voltage sources. In many cases this approach is more convenient since the nodal analysis often forces to introduce the source resistance R_X from nowhere to be able to make the necessary signal source transforms. Figure 4 illustrates the redrawn common-source circuit suitable for mesh analysis.

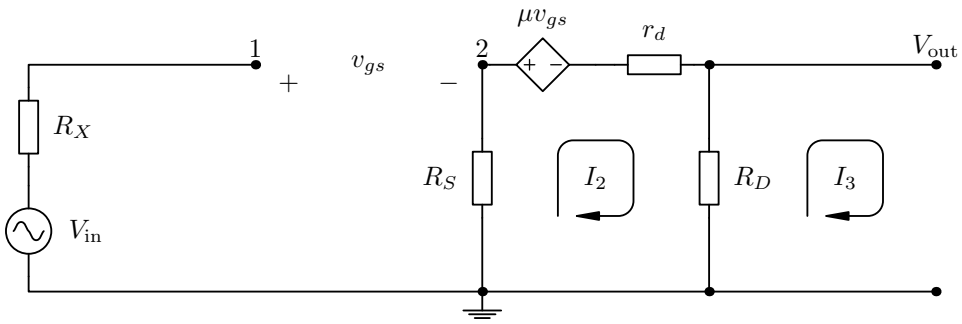


Figure 4: Mesh current model of the common-source amplifier

Since the first current loop is open-circuited, the output short circuit current is evaluated from the matrix equation

$$\begin{bmatrix} R_S + r_d + R_D & -R_D \\ -R_D & R_D \end{bmatrix} \times \begin{bmatrix} I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} -\mu v_{gs} \\ 0 \end{bmatrix}.$$

The voltage v_{gs} in this matrix equation can be expressed using the mesh currents as $v_{gs} = V_{\text{in}} - (-I_2 R_S)$, and therefore the matrix is reshaped to

$$\begin{bmatrix} (\mu+1)R_S + r_d + R_D & -R_D \\ -R_D & R_D \end{bmatrix} \times \begin{bmatrix} I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} -\mu V_{\text{in}} \\ 0 \end{bmatrix}.$$

The use of Cramer's rule to solve the output short circuit current I_3 leads to a solution

$$I_3 = \frac{-\mu V_{\text{in}}}{r_d + (\mu+1)R_S}.$$

Finally, the output impedance is evaluated as the quotient of $\frac{V_3}{I_3}$, which equals

$$Z_{\text{out}} = \frac{V_3}{I_3} = \frac{R_D[r_d + (\mu+1)R_S]}{R_D + r_d + (\mu+1)R_S}.$$

The small-signal model of an electron tube is very similar to the JFET model. Therefore, the equations derived for the JFET are equally applicable for the tube as well. One can just replace the drain resistor R_D with the plate resistor R_P, the internal drain resistance r_d with the internal plate resistance r_p, the source resistor R_S with the cathode resistor R_K, and the tube model is ready to be used.