Estimating the input and output impedances of active circuit networks using SPICE and Octave

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This example shows how to apply SPICE simulations and numerical analysis to estimate the input and output impedances of electric circuits. Often it is quite simple to evaluate the impedance of any passive network but when active circuit elements such as transistors are included, the concept of impedance becomes a bit more challenging to understand. The input and output impedance of amplifiers stages are meaningful when loading effects between different stages or even between different devices are considered. When voltage gain and voltage transfer are concerned it is vital to analyse the loading between circuit stages.

As a general procedure, the input and output impedances can be evaluated using a test voltage source, which is inserted between the circuit nodes where the impedance is measured. Specifically for determining the output impedance, one can also utilise the Thévenin and Norton theorems. According to these theorems, the output impedance of any circuit stage is obtained as the quotient of open-circuit voltage and short-circuit current.

Figure 1 shows the circuit for which the input and output impedances are determined in this example.

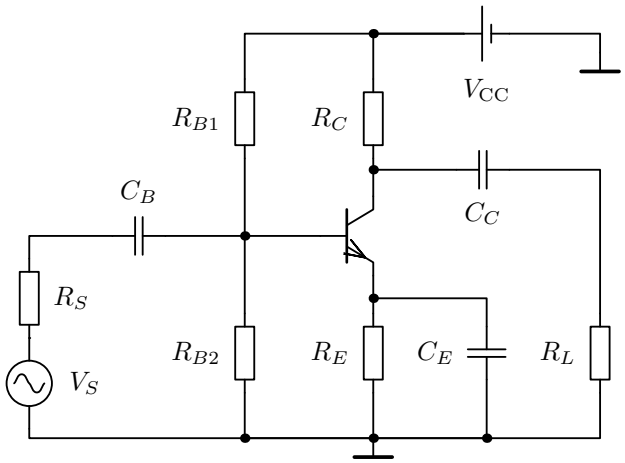

Figure 1: A common-emitter BJT amplifier

1 Impedance estimates using SPICE

Figure 2 includes a redrawn schematic of the common-emitter amplifier. The only difference compared to Figure 1 is that the signal source is named as $V_{\mathtt{test}}$ to indicate that it is only used for testing the circuit parameters.

The schematic in Figure 2 has been drawn using the `gschem` schematic editor

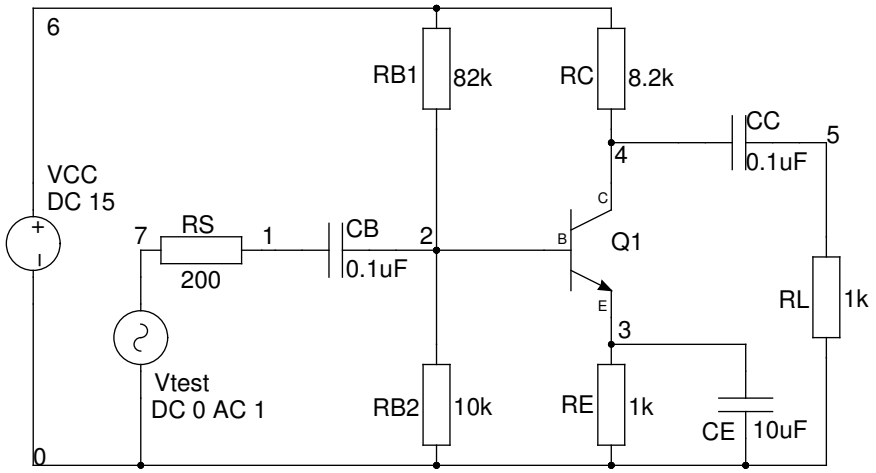

Figure 2: A common-emitter BJT amplifier with a test voltage source at the input

from the gEDA design tool package. When utilising the gEDA package, the netlist file for SPICE simulations can be created from the gschem schematic with the gnetlist application. The following snippet is a copy of the netlist file with manually added .control section, which defines the simulation commands for SPICE.

```
* gnetlist -g spice-sdb -o inputim.net inputim.sch
************************************************************
* Spice file generated by gnetlist                         *
* spice-sdb version 4.28.2007 by SDB --                    *
* provides advanced spice netlisting capability.           *
* Documentation at http://www.brorson.com/gEDA/SPICE/      *
************************************************************

.control
ac dec 90 100 100K
alter RC 1k
ac dec 90 100 100K
gnuplot inimp abs(ac1.v(7)/ac1.i(Vtest)) abs(ac2.v(7)/ac2.i(Vtest))
.endc

.OP

*==============  Begin SPICE netlist of main design ============
Vtest 7 0 DC 0 AC 1
RL 0 5 1k
```

```
VCC 6 0 DC 15
Q1 4 2 3 NPN1
.MODEL NPN1 NPN (Is=1.0e-15 Bf=181)
CE 0 3 10uF
CC 4 5 0.1uF
CB 1 2 0.1uF
RS 1 7 200
RB2 0 2 10k
RE 0 3 1k
RC 4 6 8.2k
RB1 2 6 82k
.end
```

This simulation performs a frequency sweep from 100 Hz to 100 kHz and evaluates the input impedance within this frequency range. The effect of collector resistance is investigated by evaluating the sweep with the values of $R_C = 8.2$ kΩ and $R_C = 1.0$ kΩ. Since there are frequency dependent components (capacitors) in the circuit, the input impedance will not be constant for all input signal frequencies. The input impedance is evaluated by dividing the voltage of the test source by the current flowing through the source.

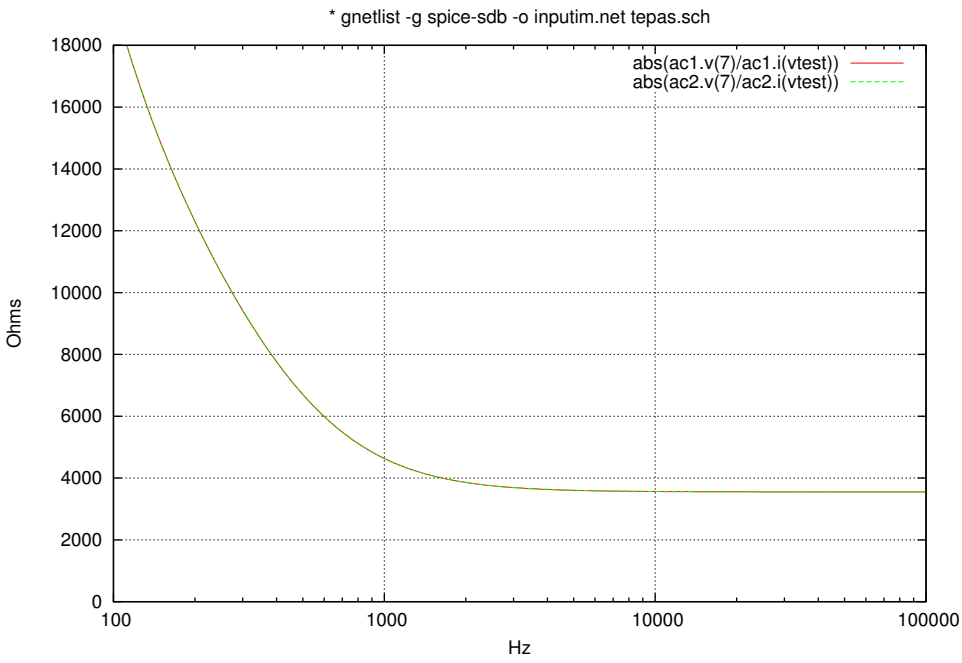

Figure 3: The simulated input impedance

The results of the simulation are shown in Figure 3. The general theory of

BJT amplifiers estimates that the input impedance of the common-emitter configuration is approximately equal to the internal input resistance r_π. The changes in the collector resistance in this example do not affect the input impedance because the value of r_π does not depend on R_C. Therefore, Figure 3 only shows one impedance curve which is overlapping the other one. The value of the input impedance indeed equals r_π at the pass-band, where the capacitors are not affecting the frequency response.

To evaluate the output impedance, the test voltage source is placed between the circuit nodes from where the impedance is to be 'measured'. The original signal source at the input side is short-circuited in this case. This configuration is shown in Figure 4, which is drawn using the `gschem` application.

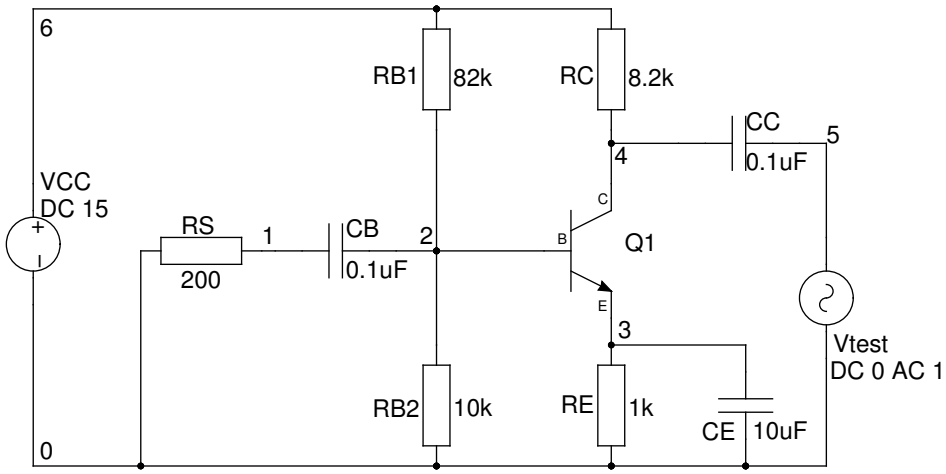

Figure 4: A common-emitter BJT amplifier with a test voltage source at the output

The output impedance setup is simulated in a similar fashion as in the case of the input impedance. The following listing is a direct copy of the complete SPICE netlist file, which is ready to be simulated as is.

```
* gnetlist -g spice-sdb -o outputim.net outputim.sch
**************************************************
* Spice file generated by gnetlist                *
* spice-sdb version 4.28.2007 by SDB --           *
* provides advanced spice netlisting capability.  *
* Documentation at http://www.brorson.com/gEDA/SPICE/   *
```

```
**********************************************************

.control
ac dec 90 100 100K
alter RC 1k
ac dec 90 100 100K
gnuplot outimp abs(ac1.v(5)/ac1.i(Vtest)) abs(ac2.v(5)/ac2.i(Vtest))
.endc

.OP


*==============  Begin SPICE netlist of main design ============
Vtest 5 0 DC 0 AC 1
VCC 6 0 DC 15
Q1 4 2 3 NPN1
.MODEL NPN1 NPN (Is=1.0e-15 Bf=181)
CE 0 3 10uF
CC 4 5 0.1uF
CB 1 2 0.1uF
RS 1 0 200
RB2 0 2 10k
RE 0 3 1k
RC 4 6 8.2k
RB1 2 6 82k
.end
```

The simulation performs a frequency sweep from 100 Hz to 100 kHz and evaluates the input impedance within this frequency range. The effect of the collector resistance is investigated by evaluating the sweep with the values of $R_C = 8.2\,\text{k}\Omega$ and $R_C = 1.0\,\text{k}\Omega$. Since there are frequency dependent components (capacitors) in the circuit, the output impedance will not be constant for all input signal frequencies. The output impedance is evaluated by dividing the voltage of the test source by the current flowing through the source.

The results of the simulation run are shown in Figure 5. The general theory of BJT amplifiers estimates that the input impedance of the common-emitter configuration is approximately equal to the collector resistance R_C. The simulated impedance curves verify that the value of the output impedance approximately equals R_C at the pass-band, where the capacitors are not affecting the frequency response.

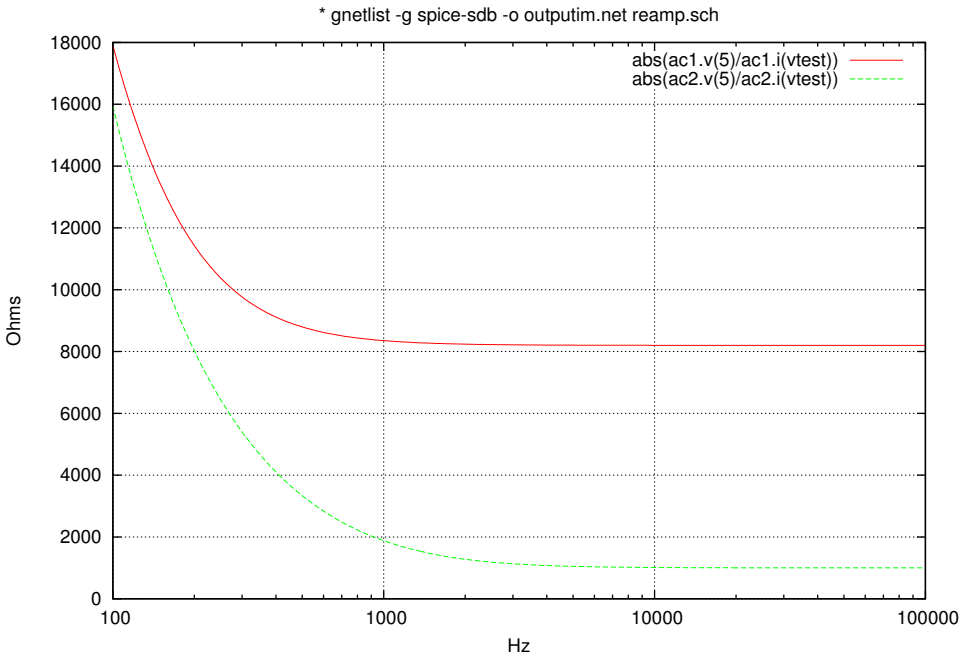

Figure 5: The simulated output impedance

2 Impedance estimates using Octave

In `Octave` one needs to first create the matrix equations that describe the small-signal models. Both models for mesh and nodal analysis need to be drawn, although in this case the mesh analysis is more important than the nodal analysis.

Figure 6 shows the small-signal model for determining the input impedance using mesh analysis. The controlled current source is transformed into a voltage source using the Thévenin and Norton theorems, which are intended to be used for these kind of source transformations. The parallel impedance branches have been combined together to minimise the amount of current loops. The impedance matrices (the numerator and denominator determi-

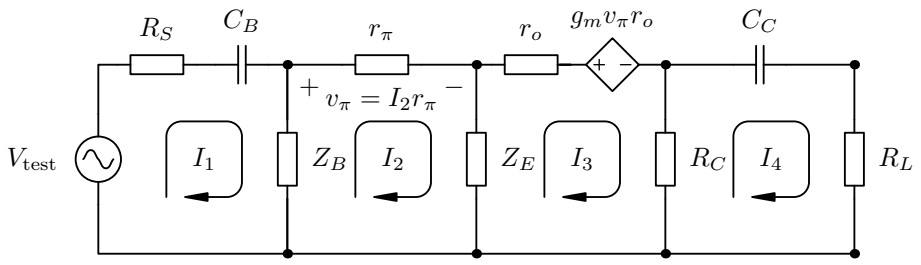

Figure 6: A small-signal model for determining the input impedance

nants) for this circuit are of the form

```
% input impedance evaluated using the test input source
ios  = [ Vtest  Z12 0   0  ; ...
         0      Z22 Z23 0  ; ...
         0      Z32 Z33 Z34; ...
         0      0   Z43 Z44];

inim = [ Z11 Z12 0   0  ; ...
         Z21 Z22 Z23 0  ; ...
         0   Z32 Z33 Z34; ...
         0   0   Z43 Z44];
```

The impedance terms in this matrix are

```
Z11 = RS + ZB + (1/(i*w*CB));
Z12 = Z21 = -ZB;
Z22 = ZB + rpi1 + ZE;
Z23 = -ZE;
Z32 = -ZE + gm*rpi1*ro;
Z33 = ZE + ro + RC;
Z34 = Z43 = -RC;
Z44 = RC + (1/(i*w*CC)) + RL;
Z444 = RC + (1/(i*w*CC));
Z54 = Z45 = -RL;
Z55 = RL;
```

The current flowing through the test source is obtained by evaluating the circulating current I_1 of the first loop. This mesh current can be calculated as

```
det(ios)/det(inim)
```

and the input impedance is therefore evaluated as

```
abs( Vtest/( det(ios)/det(inim) ) )
```

The impedance is in the complex form in general, but the total magnitude of the impedance is obtained by taking the absolute value of the impedance expression. Figure 7 shows the calculation results, which are practically the same compared to the results obtained by SPICE.

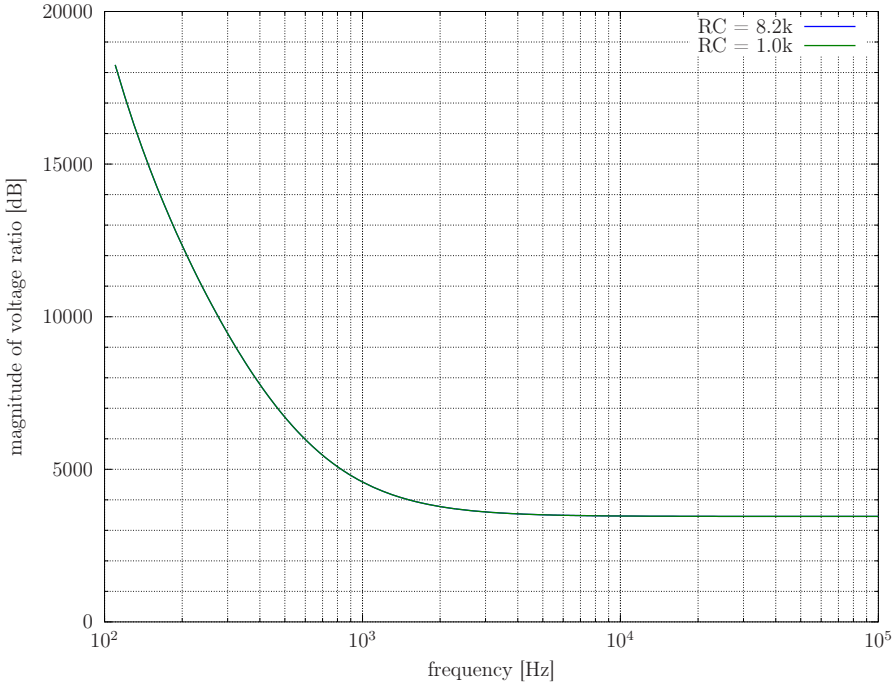

Figure 7: The simulated input impedance

When using the test source to provide the signal to the circuit, the output impedance is evaluated in a similar fashion as the input impedance. Figure 8 shows the small-signal model for determining the output impedance using mesh analysis. The test source has been placed between the output nodes of the circuit from where the impedance is evaluated. Otherwise the small-signal model is the same as in the case of the input impedance.

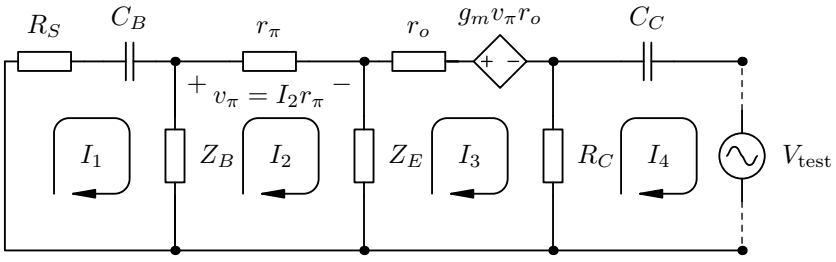

Figure 8: A small-signal model for determining the output impedance

The numerator and denominator impedance matrices derived from this circuit are of the form

```
% output impedance evaluated using the test source at output
ios2 = [ Z11 Z12 0   0; ...
         Z21 Z22 Z23 0 ; ...
         0   Z32 Z33 0 ; ...
         0   0   Z43 -Vtest];

inim2 = [ Z11 Z12 0   0  ; ...
          Z21 Z22 Z23 0  ; ...
          0   Z32 Z33 Z34; ...
          0   0   Z43 Z444];
```

The complete expressions for the impedance terms are the same as for the input impedance evaluation.

The current flowing through the test source is obtained by evaluating the circulating current I_4 of the rightmost loop. Since the evaluation is based on Cramer's rule, this mesh current can be calculated as

```
det(ios2)/det(inim2)
```

and the input impedance is therefore evaluated as

```
abs( Vtest/( det(ios2)/det(inim2) ) )
```

The results are again in good agreement with the SPICE simulations as can be seen from Figure 9. In both cases the output impedance approaches the value of the collector resistor R_C.

Alternatively, the output impedance can also be determined using the circuit analysis theorems of Thévenin and Norton. For this method one needs to evaluate also the voltage gain of the open-circuited small-signal model. The small-signal model in question is given in figure 10.

The corresponding admittance matrices (numerator and denominator determinants) for the open-circuit voltage gain are

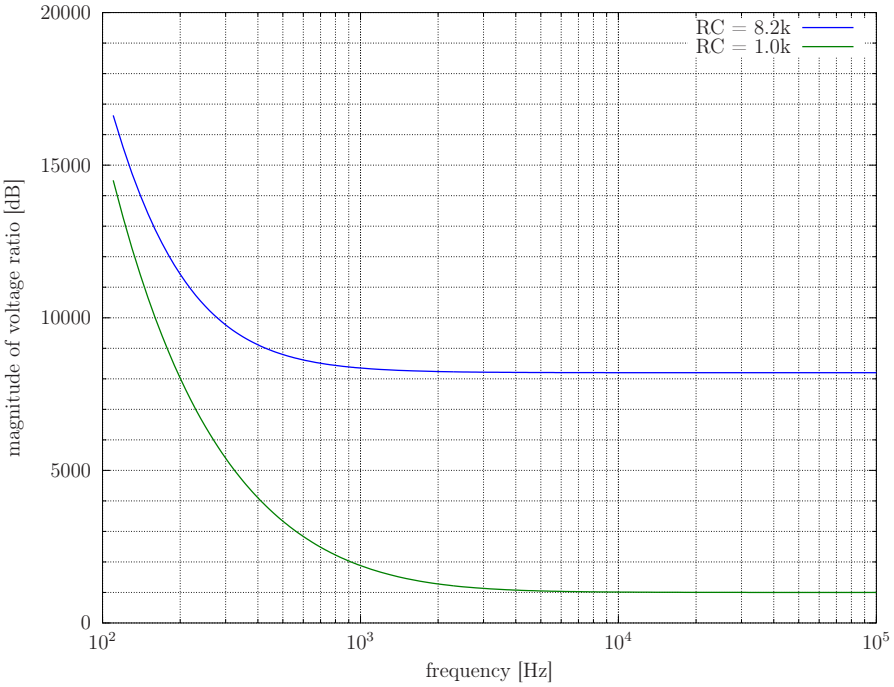

Figure 9: The simulated output impedance

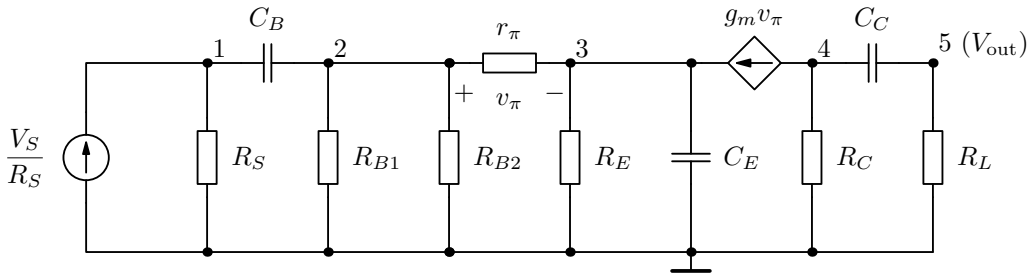

Figure 10: A small-signal model for determining the voltage gain

```
% the numerator admittance matrix (determinant), solve for column 5
osx = [ Y11 Y12 0   0   (1/RS); ...
        Y21 Y22 Y23 0   0; ...
        0   Y32 Y33 0   0; ...
        0   Y42 Y43 Y44 0; ...
        0   0   0   Y54 0];
% the denominator admittance matrix (determinant)
nimx = [ Y11 Y12 0   0   0; ...
         Y21 Y22 Y23 0   0; ...
         0   Y32 Y33 0   0; ...
         0   Y42 Y43 Y44 Y45; ...
         0   0   0   Y54 Y55x];
```

with the admittance expressions

```
Y11 = 1/RS + i*w*CB;
Y12 = Y21 = -i*w*CB;
Y22 = i*w*CB + 1/RB1 + 1/RB2 + 1/rpi1;
Y23 = -1/rpi1;
Y32 = -(B1+1)/rpi1;
Y33 = (B1+1)/rpi1 + 1/RE + i*w*CE;
Y42 = B1/rpi1;
Y43 = -B1/rpi1;
Y44 = i*w*CC + 1/RC;
Y45 = Y54 = -i*w*CC;
Y55 = i*w*CC + RL;
Y55x = i*w*CC;
```

According to Figure 6, the impedance matrices (numerator and denominator determinants) for the short-circuit current are

```
ios3  = [ Z11 Z12 0   0   Vtest; ...
          Z21 Z22 Z23 0   0; ...
          0   Z32 Z33 Z34 0; ...
          0   0   Z43 Z44 0; ...
          0   0   0   Z54 0];

inim3 = [ Z11 Z12 0   0   0; ...
          Z21 Z22 Z23 0   0; ...
          0   Z32 Z33 Z34 0; ...
          0   0   Z43 Z44 Z45; ...
          0   0   0   Z54 Z55];
```

The input impedance is therefore evaluated as

```
abs( ( det(osx)/det(nimx) )/( det(ios3)/det(inim3) ) )
```

Note that in this case a fifth current loop was added to Figure 6 to represent the actual short-circuited current loop. This alternative method yields exactly the same results as when placing a test source at the output node of the circuit.